

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 55-133574

(43)Date of publication of application : 17.10.1980

(51)Int.Cl.

H01L 29/78
H01L 29/06
H01L 29/60

(21)Application number : 54-041411

(71)Applicant : NEC CORP

NIPPON TELEGR & TELEPH
CORP <NTT>

(22)Date of filing : 05.04.1979

(72)Inventor : ICHIKAWA TETSUO

HIDESHIMA KENJI

SATO HIDEYOSHI

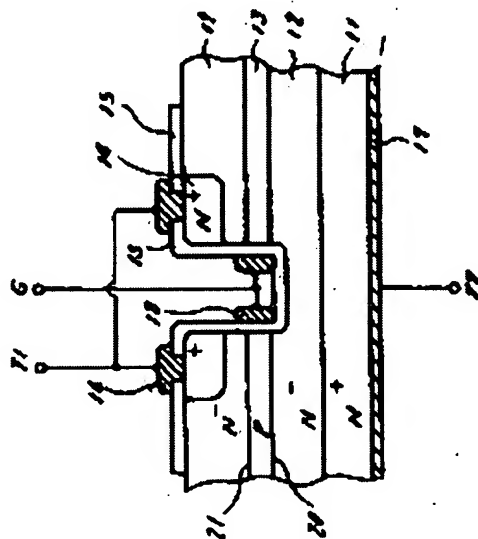
SHIMADA YUKI

(54) INSULATED GATE FIELD EFFECT TRANSISTOR

(57)Abstract:

PURPOSE: To provide a high speed switching characteristic at an insulated gate field effect transistor and control the power of the transistor in bidirectional direction by forming an insulated gate on the recess surface to form a channel forming region thereon.

CONSTITUTION: A low impurity density n-type region 12 is formed on an n-type high impurity density silicon semiconductor substrate 11, a p-type channel forming region 13 is formed in contact with the region 12, an n-type region is so formed in contact with the region 13 to become low impurity density, and an n+-type region 14 to become n-type high impurity density is formed in the region 19. A recess is then formed on the surface to reach the region 12, and an oxide film 15 and metal electrodes 16, 17 and 18 are formed thereon.



LEGAL STATUS